Modeling and Small-Signal Analysis of Controlled On-Time Boost Power-Factor-Correction Circuit

Byungcho Choi, Member, IEEE, Sung-Soo Hong, and Hyokil Park

Abstract—A large-signal average model for the controlled on-time boost power-factor-correction (PFC) circuit is developed and subsequently linearized, resulting in a small-signal model for the PFC circuit. AC analyses are performed using the small-signal model, revealing new results on the small-signal dynamics of the PFC circuit. The analysis results and model predictions are confirmed with experimental measurements on a 200-W prototype PFC circuit.

Index Terms—Average model, controlled on-time boost power-factor-correction circuit, small-signal modeling and analysis.

I. INTRODUCTION

THE controlled on-time boost power-factor-correction (PFC) circuit [1], [2] has been widely used for low-power applications, however, research results on the modeling and dynamic analysis of the PFC circuit are limited. There is no existing report on an average model that predicts the time-domain dynamics of the PFC circuit. Accordingly, when studying the large-signal transient behavior of the PFC circuit, reliance is placed on a discrete-time model that requires excessive computational time. Furthermore, since the high-frequency small-signal model for the controlled on-time boost PFC circuit has not been presented as yet, a low-frequency small-signal model derived from the power balance condition [3] has been used for the analysis and design of the PFC circuit. However, this paper will show that the existing low-frequency model is inaccurate in predicting the phase characteristics of the PFC circuit. Accordingly, a control design based on the low-frequency model can overestimate the phase margin of the PFC circuit. This inaccuracy of the low-frequency model can overestimate the phase margin of the PFC circuit. This inaccuracy of the low-frequency model becomes increasingly consequential when the control bandwidth of the PFC circuit expands with the employment of auxiliary means of removing low frequency ripple from the output voltage, for example, the addition of a notch filter in the control loop [2].

This paper proposes dynamic models for the controlled on-time boost PFC circuit and presents new results obtained from small-signal analyses using the proposed models. First, an average model is proposed that predicts the averaged time-domain behavior of the PFC circuit. When implemented with a general purpose circuit simulator such as PSpice, this average model significantly reduces the simulation time while preserving the accuracy of a discrete-time model. Secondly, a small-signal model that overcomes the inaccuracy of the existing low-frequency model is obtained by linearizing the average model. Finally, the ac dynamics of the PFC circuit are investigated using this small-signal model. It will be shown that the control-to-output transfer function of the PFC circuit contains a pole–zero pair that is located at the same distance from the origin yet on opposite sides of the $s$ plane. This pole-zero pair causes an additional $180^\circ$ phase delay and critically influences the phase characteristics of the PFC circuit. The analysis results and model predictions are verified by frequency- and time-domain simulations and experimental measurements on a 200-W prototype PFC circuit.
II. LARGE-SIGNAL AVERAGED MODEL

Fig. 1(a) shows a schematic diagram of the controlled on-time boost PFC circuit [1], [2]. Fig. 1(b) shows the major waveforms of the PFC circuit assuming that the rectified line voltage $v_{\text{L}}$, output voltage $v_{\text{O}}$, and control voltage $v_{\text{C}}$, remain constant within each switching period $T_S$. Initially, the PFC circuit assumes an on-time operation where the MOSFET is on and the ramp signal, $v_{\text{ramp}}$, increases with the slope of $s_c$. When the $v_{\text{ramp}}$ reaches the control voltage $v_{\text{C}}$, the comparator resets the latch and the PFC circuit commences the off-time operation by turning the MOSFET off and resetting the $v_{\text{ramp}}$. When the inductor current is reduced to zero, the zero-current detector sets the latch and the PFC circuit resumes its on-time operation.

A. Average Model for Power Stage

The first step in developing an average model for the power stage is to formulate a set of time-averaged equations for the voltages and currents associated with the subcircuit that alters its structure during each switching interval [4]–[6]. The subcircuit that changes its structure during the circuit operation can be identified as an active–passive switch pair combined with an inductor, as shown in Fig. 2. Referring to Figs. 1(b) and 2, the instantaneous voltage across the inductor $v(t)$ can be given as

$$v(t) = \left\{ \begin{array}{ll} v_{\text{C}}(t^*), & t \leq t^* < t + dT_S \\ v_{\text{C}}(t^*) - v_{\text{pe}}(t^*), & t + dT_S \leq t^* < t + T_S \end{array} \right. \quad (1)$$

where $t$ represents the time instant at which the PFC circuit initiates its on-time operation and $t^*$ denotes the instantaneous time. The time-averaged expression for the voltage across the inductor $V_{\text{av}}(t)$ can be given by

$$V_{\text{av}}(t) = \frac{1}{T_S} \left[ \int_{t}^{t+dT_S} v_{\text{av}}(t^*) dt^* \right]$$

$$+ \frac{1}{T_S} \left[ \int_{t+dT_S}^{t+T_S} (v_{\text{C}}(t^*) - v_{\text{pe}}(t^*)) dt^* \right] \quad (2)$$

that can be simplified as

$$V_{\text{av}}(t) = V_{\text{C}}(t) - (1 - d)V_{\text{pe}}(t) \quad (3)$$

where $V_{\text{C}}(t)$ and $V_{\text{pe}}(t)$ represent the time-averaged value for the respective voltages, and $d$ represents the duty ratio of the active switch. Equation (3) assumes that $|v_{\text{pe}}(t^*) - V_{\text{pe}}(t)| \ll |V_{\text{C}}(t)|$ for each switching interval. The averaged expression for the voltage across the switch can be obtained by

$$V_{\text{ba}}(t) = V_{\text{av}}(t) + V_{\text{C}}(t) \quad (4)$$

From (3) and (4), a time-averaged equation for $v_{\text{ba}}(t)$ and $v_{\text{pe}}(t)$ can be written as

$$v_{\text{ba}}(t) = (1 - d)v_{\text{pe}}(t) \quad (5)$$

By applying the power balance condition to Fig. 2, it follows that

$$V_{\text{ba}}(t)I_L(t) = V_{\text{pe}}(t)I_p(t) \quad (6)$$

which can be simplified as

$$I_p(t) = (1 - d)I_L(t) \quad (7)$$

where $I_p(t)$ and $I_L(t)$ represent the time-averaged value of the associated currents. Equations (5) and (7) describe the time-averaged dynamics of the subcircuit.

B. Average Model for Modulator

The average model for the modulator defines the functional relationship between the duty ratio $d$ and circuit variables involved in determining the state of the switches. Referring to Fig. 1(b), the slope of the ramp signal $s_c$ can be written as

$$s_c = \frac{v_{\text{C}}}{dT_S} \quad (8)$$

and the on-time slope $s_n$ and off-time slope $s_f$ of the inductor current can be given as

$$s_n = \frac{v_{\text{L}}}{L} \quad (9)$$

$$s_f = \frac{(v_{\text{C}} - v_{\text{L}})}{L}. \quad (10)$$

It can be seen from Fig. 1(b) that

$$s_n dT_S = s_f (1 - d)T_S \quad (11)$$

which simplifies to

$$(s_n + s_f)d = s_f. \quad (12)$$

Referring to Fig. 1(b), the time-averaged value of the inductor current can be found to be

$$i_L = 0.5 \left( s_n d^2 + s_f (1 - d)^2 \right) T_S \quad (13)$$

by directly averaging the instantaneous value of the inductor current. By incorporating (8)–(10) and (12) into (13) and simplifying the resulting equation, the following equation can be obtained:

$$v_{\text{C}}d \left( d + \frac{2s_n i_L}{v_{\text{pe}}} - 1 \right) = 0 \quad (14)$$

which gives an expression for the duty cycle as

$$d = 1 - \frac{2s_n i_L}{v_{\text{pe}}} \quad (15)$$

An average model for an entire PFC circuit can be obtained by programming (5), (7), and (15), along with other parts of the circuit, using a general purpose circuit simulator. Fig. 3 shows a circuit representation of the averaged model implemented with PSpice. In the PSpice program, (5) and (7) are transformed into an ideal transformer and (15) is coded as a functional equation. The listing of the PSpice code is given in Fig. 11. Fig. 4 presents a comparison between the predictions of the average model and the results of exact cycle-by-cycle simulations using Saber [7].
The response of the average model during transition periods will be demonstrated in Section IV.

III. SMALL-SIGNAL MODELING AND ANALYSIS

A small-signal model of the PFC circuit can be obtained, in principle, by linearizing the average model. However, unlike cases for dc-to-dc converters, operating conditions of PFC circuits vary extensively within each line period. This substantial change in the operating point has presented difficulties in the development of small-signal models for PFC circuits. One simple solution to this problem is to consider PFC circuits as dc-to-dc converters with an equivalent dc input that corresponds to the rms value of the rectified line voltage. References [8]–[10] confirmed the validity of this approach. By adapting the aforementioned approximation to the average model developed in the previous section, this section presents a small-signal model for the controlled on-time boost PFC circuit.

A. Small-Signal Model for Power Stage

Assuming the input of the power stage is a dc voltage identical to the rms value of the rectified line voltage, (5) and (7) can be linearized to produce equations relating the ac components of the circuit variables

\[ \hat{v}_{oa} = (1 - D) \hat{v}_{oa} - V_{oa} \hat{d} \]  
\[ \hat{i}_{d} = (1 - D) \hat{i}_{L} - I_{L} \hat{d} \]

with \( D = (V_{O} - V_{\text{rms}})/V_{O} \), \( V_{oa} = V_{O} \), and \( I_{L} = I_{O}/(1 - D) \) where \( V_{O} \) is the average value of the output voltage, \( I_{O} \) is the average value of the load current, and \( V_{\text{rms}} \) represents the rms value of the rectified line voltage.

B. Small-Signal Model for Modulator

By linearizing (15), the small-signal duty ratio, \( \hat{d} \), can be expressed as a linear combination of the small-signal components of the circuit variables associated with the average model of the modulator

\[ \hat{d} = \frac{1 - D}{V_{C}} \hat{v}_{c} + \frac{1 - D}{V_{O}} \hat{v}_{o} - \frac{2L_{s}e}{V_{C}V_{O}} \hat{i}_{L} \]

with

\[ V_{C} = \frac{2L_{s}eI_{L}}{(1 - D)V_{O}}. \]

A small-signal circuit model of the PFC circuit can, therefore, be obtained by converting (16)–(18) into linear circuit models, and subsequently combing the resulting models with the remaining part of the PFC circuit. Fig. 5 presents a circuit representation of the small-signal model that can be programmed with a general purpose circuit simulator.

C. Control-to-Output Transfer Function

An analytical expression for the control-to-output transfer function of the PFC circuit is derived, thereby, addressing the difference between the new transfer function and the existing low-frequency model.
From the small-signal model of Fig. 5, the following equations can be easily seen:

\[
\hat{v}_o = \frac{R(1+sC R_c)}{1+sC(R+R_c)} \hat{v}_o \tag{20}
\]

\[
\hat{v}_o = (1-D)\hat{i}_L - \frac{V_o}{R(1-D)} \hat{i}_o \tag{21}
\]

\[
\hat{i}_L = \frac{V_o}{s L} \hat{i}_o - \frac{1-D}{s L} \hat{v}_o. \tag{22}
\]

Equation (18) can be rewritten as

\[
\hat{d} = \frac{1-D}{V_C} \hat{v}_c + \frac{1-D}{V_o} \hat{v}_o - \frac{R(1-D)^2}{V_o} \hat{i}_L. \tag{23}
\]

As shown in the Appendix, (20)–(23) can be simultaneously solved to yield an expression for the control-to-output transfer function

\[
\frac{\hat{v}_o}{\hat{v}_c} = \frac{V_o}{V_C (2+sC(R+2R_c))} F_{pc}(s) \tag{24}
\]

where

\[
F_{pc}(s) = \frac{\left(1-s \frac{L}{R(1-D)^2}\right)}{\left(1+s \frac{L}{R(1-D)^2}\right)}. \tag{25}
\]

The $F_{pc}(s)$, a polynomial consisting of the right-half-plane (RHP) zero and left-half-plane pole (LHP) located at the same frequency, does not affect the magnitude of $\hat{v}_o/\hat{v}_c$ yet introduces a $180^\circ$ phase delay around $\omega_{pc} = \frac{R(1-D)^2}{L}$. The presence of $F_{pc}(s)$ in $\hat{v}_o/\hat{v}_c$ is the unique characteristic of the controlled on-time boost PFC circuit, that is not found in other PFC circuits or dc-to-dc converters.

It can be shown that the existing low-frequency model [3] implicitly assumes $F_{pc}(s) = 1$, and thereby incorrectly predicts the phase response of the transfer function. Fig. 6 compares the Bode plot of (24) and the control-to-output transfer function derived from the existing low-frequency model. Fig. 6(a) shows the transfer functions of the experimental PFC circuit the parameters of which are listed in the Appendix. With $L = 523 \ \mu H$ and $R = 1.44 \ \Omega$, $\omega_{pc}$ is found at $63 \ \text{kHz}$ and the effects of $F_{pc}(s)$ are exhibited at high frequencies. However, when the power stage parameters are selected differently while complying with design constraints [1], $\omega_{pc}$ could appear at relatively low frequencies. Fig. 6(b) shows the control-to-output transfer function of a PFC circuit where $L = 610 \ \mu H$ and $R = 412 \ \Omega$. In this case, a feedback compensation designed without considering the impact of $F_{pc}(s)$ could easily overestimate the stability margins of the PFC circuit. The implication of $F_{pc}(s)$ becomes increasingly significant as the control bandwidth of a PFC circuit expands with the employment of auxiliary means of removing the low frequency ripple component from the output voltage [2].

Fig. 7 shows the Bode plot of (24) and control-to-output transfer functions of the experimental PFC circuit measured with two different input conditions: one with an actual ac input and the other with a dc input corresponding to the rms value of the line voltage. There is a good agreement between analytical predictions and measured data, thereby validating the analysis results and model accuracy. In addition, the close resemblance between the transfer functions measured with an ac input and measured with a dc input justifies the validity of replacing the ac voltage with its equivalent dc value for small-signal analysis purposes [8]–[10].

D. Frequency Range for Validity of Small-Signal Model

From earlier studies [11], [12], it is known that the predictions of a small-signal model derived from an averaging technique become inaccurate as the frequency range approaches half the switching frequency. For the controlled on-time boost PFC circuit, in which the switching frequency changes considerably within each line period, the minimum switching frequency can be used to estimate the frequency range for the validity of the proposed model. It can be shown that the switching frequency, $f_s$, of the PFC circuit will vary as $70 \ \text{kHz} < f_s < 280 \ \text{kHz}$ with given power stage parameters and operating conditions [1]. Referring to Fig. 7, the gain curves of the transfer functions show a good correlation up to $30 \ \text{kHz}$, thereby confirming the general results of the averaging theory. However, the measured phase responses exhibited a lower value at frequencies above $600 \ \text{Hz}$, as compared to the model prediction. This indirectly indicates that the actual transfer function of the PFC circuit may have an additional pole at high frequencies where the proposed model fails to predict the small-signal dynamics of the PFC circuit.
Fig. 7. Control-to-output transfer functions of experimental PFC circuit. The solid line is the plot of (24), the dashed line is the measurement with an ac input, and the dotted line is the measurement with the equivalent dc input. (a) \( V_i = 160 \ V_{\text{rms}}, R = 1.44 \ \Omega \). (b) \( V_i = 200 \ V_{\text{rms}}, R = 1.44 \ \Omega \).

Fig. 8. Step load response of output voltage. (a) Experimental waveform. (b) Prediction of the average model. (c) Result of a discrete-time model implemented with Saber. The close resemblance among the waveforms demonstrates the accuracy of the average model.

Fig. 9. Step line response of output voltage. (a) Rectified line voltage. (b) Experimental waveform of the output voltage. (c) Prediction of the average model. (d) Result of a discrete-time model.

IV. ACCURACY OF MODELS

The accuracy of the average and small-signal model is demonstrated by comparing the model predictions with experimental measurements and exact cycle-by-cycle simulations. Fig. 8 shows the output voltage of the PFC circuit when a step load change from \( R = 0.7 \ \Omega \) to \( R = 1.4 \ \Omega \) occurred at \( t = 0.05 \ \text{s} \). Fig. 8(a) is the experimental waveform, and Fig. 8(b) is the result of a PSpice simulation using the average model. The average model accurately predicts the transient response as well as the 120-Hz ripple in a steady state. Fig. 8(c) shows the waveform obtained from the discrete-time model implemented with Saber [7]. Fig. 9 shows the output voltage when a step line change from \( V_i = 190 \ \text{V}_{\text{rms}} \) to \( V_i = 130 \ \text{V}_{\text{rms}} \) occurred at \( t = 0.05 \ \text{s} \). The close conformity among the experimental waveform [Fig. 9(b)], the prediction of the average model [Fig. 9(c)], and the result of the discrete-time model [Fig. 9(d)] confirms the accuracy of the average model.

Fig. 10 shows the loop gain of the PFC circuit simulated using the small-signal model of Fig. 5, in parallel with the loop gains measured with an ac input and measured with a dc input. The loop gains were measured with an HP4194A impedance analyzer using the analog modulation technique discussed in [13]. The small-signal model closely approximates the gain and phase characteristics up to high frequencies, well above 10 kHz. The transfer function measured with an ac input shows fluctuations at frequencies around 100–150 Hz. This fluctuation is due to the combined effects of the 120-Hz switching at the bridge rectifier and the 120-Hz ripple component in the output voltage.
Fig. 10. Loop gain of experimental PFC circuit. The solid line is a prediction of the small-signal model, the dashed line is the measurement with an ac input, and the dotted line is the measurement with a dc input. (a) $V_{i} = 160 \ \text{V}_{\text{rms}}, R = 1.44 \ \text{k} \Omega$. (b) $V_{i} = 200 \ \text{V}_{\text{rms}}, R = 1.44 \ \text{k} \Omega$.

V. CONCLUSIONS

In spite of its widespread use, the controlled on-time boost PFC circuit has not received much research attention, particularly in the area of the modeling and small-signal analysis. One reason for this might be a general conception that the existing low-frequency model would be adequate for analysis and design purposes. The conception might be justified for cases of standalone PFC circuits with a narrow control bandwidth, however, for PFC circuits with a wide control bandwidth or PFC circuits for distributed power applications, a small-signal model which is accurate at frequencies from dc to high-frequency band is a prerequisite for ac analyses and control design.

This paper has presented a high-frequency small-signal model for the controlled on-time boost PFC circuit that overcomes the inaccuracy of the existing model. The ac characteristics of the PFC circuit were then investigated using the proposed small-signal model. It was shown that the control-to-output transfer function of the PFC circuit includes an RHP zero and LHP pole located at the same frequency. This pole-zero pair could appear at relatively low frequencies, and critically affect the phase characteristics of the PFC circuit. In addition, this paper presented an average model that can predict the averaged time-domain dynamics of the controlled on-time boost PFC circuit. This average model can be used as an alternative to the costly discrete-time model when studying the large-signal transient behavior of the PFC circuit.

Average model for boost PFC circuit

********** Parameters **********

.PARAM FLINE = 60
.PARAM VIN = 160
.PARAM FS = 98E3
.PARAM L = 322.7U
.PARAM ILO = 0
.PARAM CO = 235U
.PARAM PO = 200
.PARAM VO = 380
.PARAM SE = 274725.275

******** Input and output stage ********

.EVREF 12 0 DC 5
.EVO V1 0 3 0 1
.RA V1 11 752K
.RB 11 0 10K
.R2 11 14 73K
.C2 14 13 0.089U
.REA 13 0 1G
.ED1 5 0 TABLE [1 - 2*L*I(VD2)*SE/V(3)/V(13)] = 0.0 1.1
.RD1 5 0 1G
.OPTIONS ITL5 = 0 RELTOL = 0.1 VNTOL = 1U
+ ABSTOL = 1PA
.TRAN 0.1m 100m 0U 50U UIC
.MODEL DMOD D
.MODEL SMOD VSWITCH(RON = 0.001)
.PROBE
.END

Fig. 11. PSpice code for average model of PFC circuit.
APPENDIX

A. Parameters of Experimental PFC Circuit

- Input and output voltage: $V_i = 110-220$ V, $V_o = 380$ V.
- Power stage parameters: $L = 323 \mu$H, $C = 235 \mu$F, $R_c = 0.2 \Omega$, and $R = 0.723 - 1.44 \kOmega$.
- Slope of ramp signal: $S_r = 27 \times 10^5$ V/S.
- Voltage feedback compensation: $R_f = 750 \kOmega$, $R_s = 10 \kOmega$, $R_2 = 73 \kOmega$, and $C_f = 0.089 \mu$F.
- $F_v(s) = -15(1 + s/154)/s$.

B. Control-to-Output Transfer Function

Combining (20)–(22) yields
\[
\frac{1 + sC(R + R_c)}{R(1 + sCR_c)} \frac{V_o}{\hat{d}} = \frac{(1-D)V_o}{sL} \frac{(1-D)^2}{sL} \frac{V_o}{R(1-D)} \hat{d}
\]
that can be simplified as
\[
\hat{d} = 1 - \frac{D}{V_o} \frac{V_o}{(1-D)^2(1+sCR_c)} \frac{1}{(R(1-D)^2 - sL) \hat{v}_o}.
\]
Combining (22) and (23) yields
\[
\frac{sL + R(1-D)^2}{sL} \hat{d} = \frac{(1-D)\hat{v}_c}{V_C} + \frac{(1-D)(sL + R(1-D)^2)}{V_o} \frac{\hat{v}_o}{sL}.
\]
Finally, by incorporating (27) into (28) and simplifying the resulting equation, the control-to-output transfer function given by (24) is obtained.

C. PSpice Code for Average Model of PFC Circuit

See Fig. 11.

REFERENCES


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